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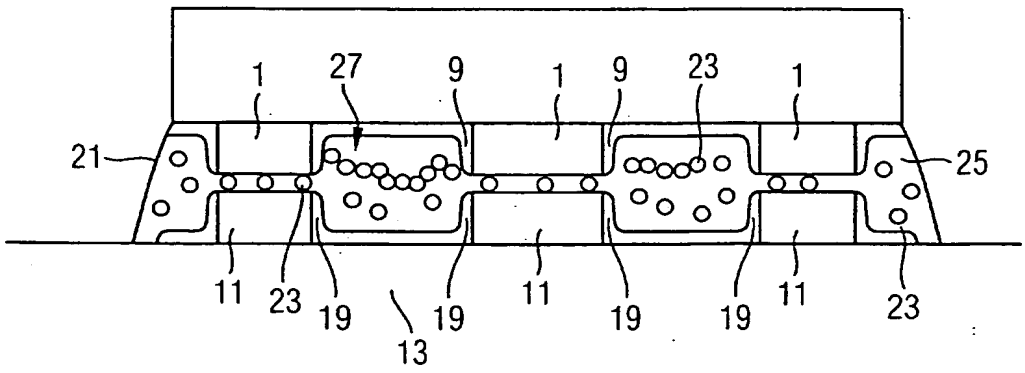
(54) Title: ATTACHMENT OF FLIP-CHIPS TO SUBSTRATES



(57) Abstract: In a method of attaching a flip chip 3 to a substrate 13, insulating layers 9, 19 are formed on the lateral sides of the electrical contacts 1 of the flip chip 3 and the lateral sides of he electrical contacts 11 of the substrate 13. The flip-chip 3 is joined to the substrate 13 by a matrix 21 of insulating material 25 including electrically conductive particles 23. The insulating layers 9, 19 reduce the risk of the formation of horizontal conducting paths between the electrical contacts 1, 11.

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Attachment of flip-chips to substrates

Field of the invention

The present invention relates to methods for attachment of flip-chips to substrates, and to flip-chips attached to substrates using the method. The term "substrate" is used in this document in a general sense to include any body onto which a flip-chip is secured, for example a printed circuit board.

Background of Invention

"Flip-chips" are integrated circuits formed with electrical contacts on one surface. The flip-chip is electrically connected to a substrate by positioning it with this surface facing a surface of the substrate. The substrate has electrical contacts at locations on that surface corresponding to the locations of the electrical contacts on the flip-chip.

The known connection scheme is shown in Fig. 1. The contacts 1 on the flip chip 3 are conventionally Au (gold) bumps in register with electrical contacts 11 on the substrate 13. The flip-chip 3 is fixed to the substrate by a paste or film layer 21. A paste layer is generally dispensed whereas a film layer is laminated onto the substrate 13. One possibility would be to form the paste or film layer 21 entirely of an insulating material, so that the layer is a non-conductive paste (NCP) or non-conductive film (NCF). However, this causes a risk of that an insulating layer is formed between certain of the bumps 1 and the contacts 11. To prevent this risk, the paste or film 21 may include conducting particles 23. The idea is that some of the conducting particles 23 are trapped between the bumps 1 and the contacts 11, and so form reliable conducting paths in the vertical direction, without such paths existing in the horizontal direction. Such horizontal paths would be disadvantageous, because they would cause lateral shorting between adjacent bumps 1 or contacts 11. For this reason, the paste including the conductive particles is

referred to as an ACP (anisotropic conductive paste) or ACF (anisotropic conductive film).

However, with the continuous shrinking of the dimensions of the electronic packaging components, the sizes of the bumps 3, of the contacts 5, and of the spaces between them in the plane of the surfaces, must be reduced. As this happens, there is an increasing risk that a configuration of the conductive particles 23 is produced which results in electrical shorting in the horizontal direction. This risk increases as the pitch (i.e. the lateral spacing of the bumps and contacts) becomes smaller, yet it would be highly expensive to reduce the size of the conductive particles further.

Summary of the Invention

The present invention aims to provide a new and useful methods for attaching a flip-chip to a substrate and combinations of a flip-chip and substrate formed by the method.

In general terms, the invention proposes that insulating layers are formed on the lateral surfaces of the electrical contacts on the flip-chip and/or on the substrate. This has the advantage that, when the flip-chips are attached to the substrate, the chance of an electrical path being formed in the lateral direction between the contacts is very much reduced.

Preferably, the insulating layer on the lateral sides of the flip-chip electrical contacts is produced by forming an insulating film over the surface of the flip-chip having the electrical contacts, and then removing the portions of the film overlying the electrical contacts by a polishing method.

Preferably, the insulating layer on the substrate is produced by coating a photo-sensitive film onto the substrate, and irradiating selected portions of the surface (e.g. with UV radiation) to modify the material properties of the layer,

such that the material overlying the contact portions can be removed selectively.

Note that it is not presently preferred to use such an irradiation technique to form the lateral films on the contacts of the flip-chip, since the flip chip may be damaged by the irradiation. Conversely, the polishing technique is not presently preferred for forming the lateral films on the contacts of the substrate, since the irradiation technique is a more mature technology, and for example does not require the electrical contacts on substrate to be formed with such a uniform height.

Brief Description of The Figures

Preferred features of the invention will now be described, for the sake of illustration only, with reference to the following figures in which:

Fig. 1 shows the attachment of a flip-chip to a substrate according to a known method;

Fig. 2, which consists of Figs. 2(a) to 2(c), shows the formation of lateral layers on the electrical contacts of a flip-chip in a method which is an embodiment of the invention;

Fig. 3, which consists of Figs. 3(a) to 3(c), shows the formation of lateral layers on the electrical contacts of a substrate in the embodiment of Fig. 2; and

Fig. 4, shows the steps of attachment of the flip-chip and circuit-board formed as shown in Figs. 2 and 3.

Detailed Description of the embodiments

The embodiment is described with reference to Figs. 2 to 4, which use equal references numerals to those used in Fig. 1 to label equivalent items. None of

these figures is drawn to scale. Referring firstly to Fig. 2, a method is shown of forming lateral layers on the electrical contacts 1 of a flip-chip 3 in the embodiment of the invention.

In a first step, as shown in Fig. 2(a), an insulating organic polymer layer 5 is formed over the surface of the flip-chip 3 carrying the electrical contacts 1 (Au bumps). The layer 5 is typically 5 to 10 micrometers thick. After it is formed, it is cured by irradiation with a lamp 7.

As shown in Fig. 2(b), the top portions of the layer 5 (i.e. the portions which overlie the electrical contacts 1) are then removed using a chemical-mechanical polishing (CMP) or "backlapping" tool 6, to give the result shown in Fig. 2(c), in which the electrical contacts 1 having insulating layers 9 on their lateral surfaces.

Turning now to Fig. 3, a method is shown of forming lateral layers on the electrical contacts 11 of a substrate 13 in a method according to the invention.

In a first step, shown in Fig. 3(a), a layer 15 of a photosensitive insulating material is coated over the surface of the substrate 13 carrying the electrical contacts 11.

In the next step, shown in Fig. 3(b), a mask 14 is positioned over the substrate 13 with masking portions 16 in register with the electrical contacts 11. The layer 15 is irradiated with a UV lamp 17 through the mask 14, so as to crosslink and harden the material which is not protected by the masking portions 16. The masking portions 16 mask the portions of the layer 15 on top of the electrical contacts 11, so these portions of the layer are not exposed to the UV light and will not crosslink. These portions of the layer 15 can now be removed by etching, to leave the structure shown in Fig. 3(c), including electrically insulating layers 19 on the lateral surfaces of the electrical contacts 11.

Turning now to Fig. 4, the flip-chip 3 produced as shown in Fig. 2 is connected to the substrate produced in Fig. 3, by a matrix 21 (ACF/ACP layer) containing electrically conductive particles 23 within an insulating material 25. The conductive particles 23 sandwiched between the electrical contacts 1, 11 provide conducting paths between the corresponding contacts in the vertical direction. Even if there are horizontal conducting paths 27 formed by the conductive particles 23, there is little or no risk of electrical shorting between horizontally (laterally) spaced apart electrical contacts 1, 11 due to the insulator layers 9, 19.

Many variations of the embodiment are possible within the scope of the invention as will be clear to a skilled reader. For example, in one variation the method of forming lateral films explained in Fig. 3 with reference to forming lateral insulating layers 19 on the contacts 11 of the substrate 13 could be used to produce the lateral insulating layers on the electrical contacts 1 of the flip-chip 3. However, it would be less straightforward to adapt the technique for forming lateral insulating layers shown in Fig. 2 to the formation of lateral insulating layers on the contacts 11 of the substrate 13.

Claims

1. A method of attaching a flip-chip to substrate, the method including forming an insulating layer of an insulating material on the lateral sides of the electrical contacts of the flip-chip and the substrate, and joining the flip-chip to the substrate using a matrix of insulating material including conductive particles.

2. A method according to claim 1 in which the insulating layer on the lateral sides of the electrical contacts of the flip-chip is formed by coating a layer of insulating material onto the surface of the flip-chip including the electrical contacts, curing the layer, and then removing the portions of the layer overlying the electrical contacts by polishing.

3. A method according to claim 1 or claim 2 in which the insulating layer on the lateral sides of the electrical contacts of substrate is formed by coating an layer of insulating material onto the surface of the substrate including the electrical contacts, exposing portions of the layer which do not overlie the electrical contacts to electromagnetic radiation to cure it, and then removing the uncured portions of the layer to expose the electrical contacts.

4. A combination of a flip-chip and a substrate, the flip-chip being oriented with a surface of the flip-chip including electrical contacts facing a surface of the substrate including corresponding electrical contacts, the electrical contacts of the flip-chip and substrate having electrically insulting films on their lateral sides, the combination further including between the flip-chip and the substrate a matrix of insulating material including electrically conductive particles.

FIG 1

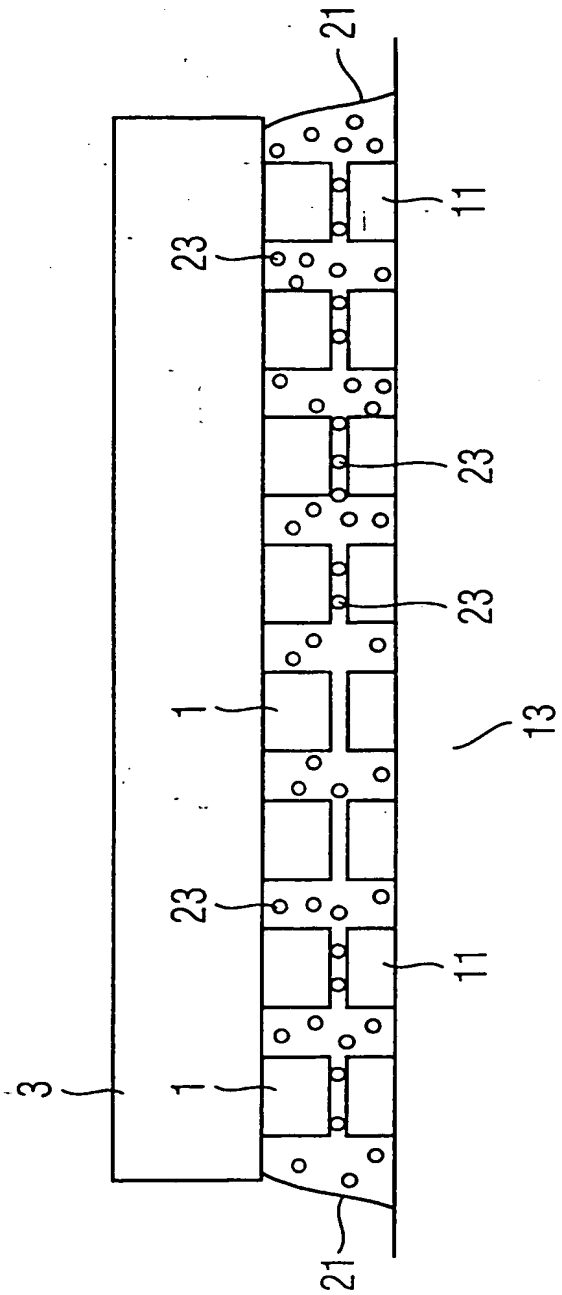


FIG 2A

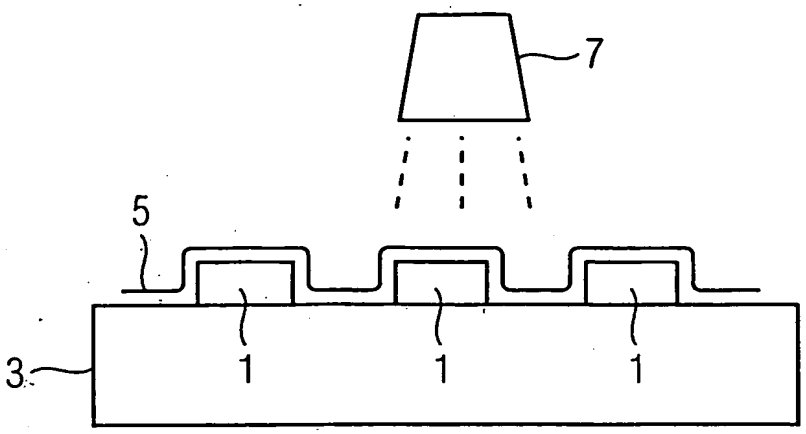


FIG 2B

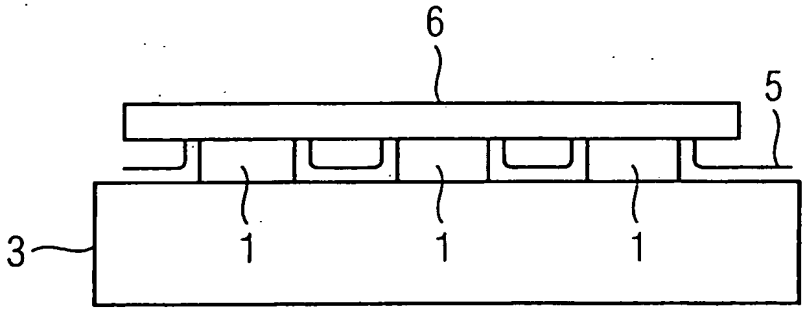


FIG 2C

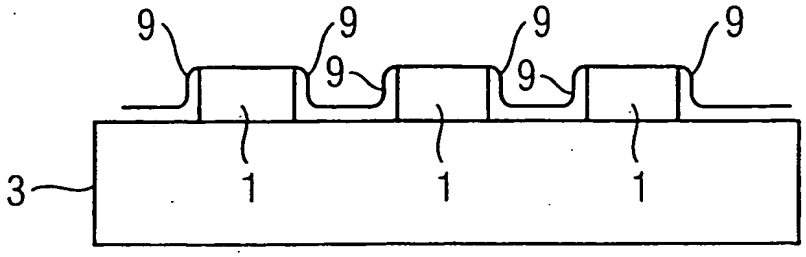


FIG 3A

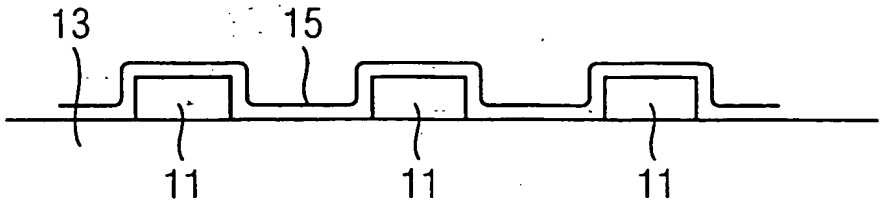


FIG 3B

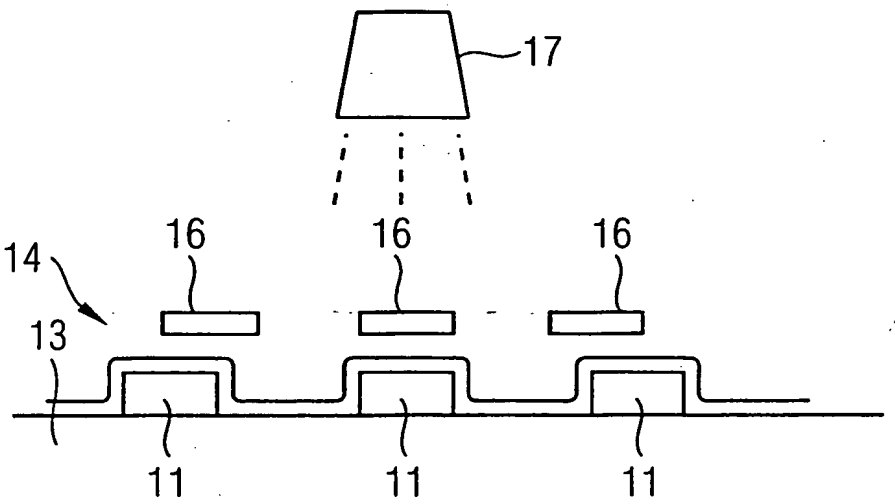


FIG 3C

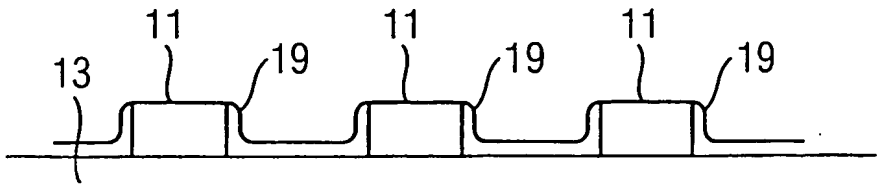
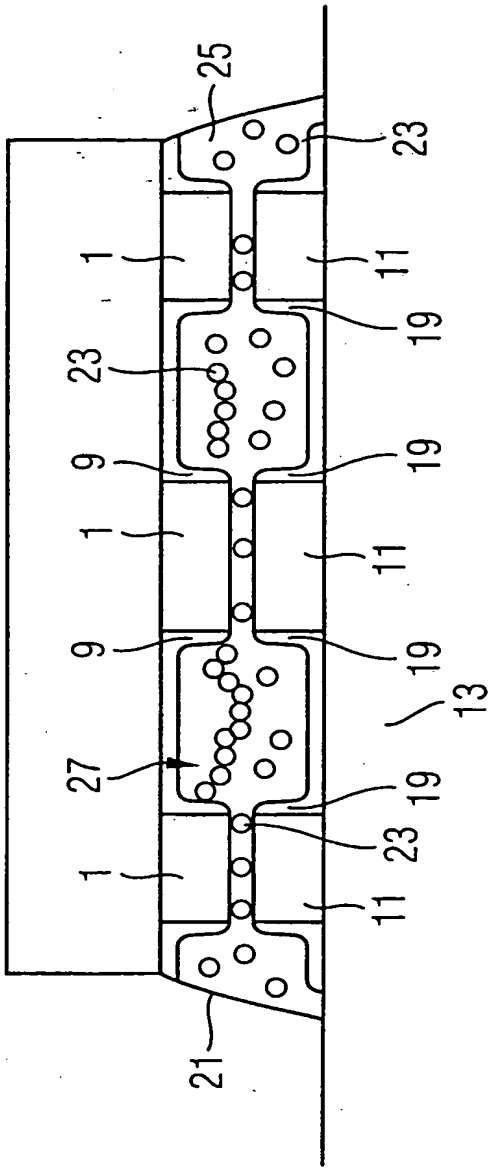


FIG 4



INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	paragraph '0023! - paragraph '0026! claims 1-8,11,15,16,19 figures 3A-6B	2,3

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA	Authorized officer
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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